REMARKS/ARGUMENT

Claims 1-10 are pending in this application. Claims 1-10 stand rejected. In light of the remarks set forth below, Applicants respectfully submits that each of the pending claims is in immediate condition for allowance.

Paragraph 6 of the Office Action responds to Applicants' previous amendment filed December 10, 2002. The Examiner states that "since a printed circuit board in its broadest definition is an insulating substrate on which circuits are mounted, Agarwala, et al. (U.S. Patent No. 5,268,072) discloses the claimed limitations. In Figure 1e, Agarwala, et al. shows an insulating substrate 15 on which circuits 16 are mounted, which meets the limitation of a printed circuit board in its broadest definition." Office Action at 4.

Applicants disagree with the Examiner's characterization of Agarwala. Layer 15, which the Examiner calls an insulating substrate, is in fact a passivating layer. (Col. 3, lns. 2-16.) A passivation layer is not a substrate. A substrate is a mechanical insulating support upon which a device is fabricated or the base for an integrated circuit or transistor. See, e.g., http://www.twysted-pair.com/dicts.htm (sub·strate; noun ; electronic engineering semiconductor crystal used as base: a single crystal of a semiconductor used as the basis for an integrated circuit or transistor); see also, http://encarta.msn.com/encnet/features/dictionary/DictionaryResults.aspx?search=substrate. A

passivating layer is a layer that makes the underlying layer inert or less reactive. Thus, it would be inappropriate to state that a passivation layer is a support upon which a circuit can be built.

In the Agarwala reference, the substrate (unnumbered) is the layer that is beneath the conductor 16. The passivation layer 15, which is above conductor 16, leaves certain areas of conductor 16 exposed so that a solder pad comprising layers 13, 14 and 18 can serve as the connection point for a solder ball 17. Clearly, therefore, since Agarwala already discloses a substrate (unnumbered), it is improper for the Examiner to construe Agarwala's passivation layer 15 as a substrate.

Applicants claim a printed circuit board 1 as the substrate. The substrate 1 has a via through the entire substrate. The conductor 3 is on the far side of the substrate while the solder ball 5, connected to the conductor 3, is connected through the via using solder pad 2. Thus, Applicants' invention is unlike the apparatus disclosed in Agarwala.

Claims 1-3, 5, 6, and 8-10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Agarwala Patent.

To anticipate a claim under 35 U.S.C. § 102, the cited reference must disclose every element of the claim, as arranged in the claim, and in sufficient detail to enable one skilled in the art to make and use the anticipated subject matter. See, PPG Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566 (Fed. Cir. 1996); C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349 (Fed. Cir. 1998). A reference that does not expressly disclose all of the

elements of a claimed invention cannot anticipate unless all of the undisclosed elements are inherently present in the reference. See, Continental Can Co. USA v. Monsanto Co., 942 F.2d 1264, 1268 (Fed. Cir. 1991).

Among the limitations of claim 1 neither shown nor inherent in Agarwala is "a pad formed on a first side of said printed circuit board ... and a via formed through said printed circuit board, said via providing electrical communication between said pad and said connecting wiring."

As discussed above in response to the Examiner's arguments, Agarwala fails to show a pad formed on a first surface and a via formed through the printed circuit board providing electrical communication between a pad on a first side of the printed circuit board and the circuit board traces on the second side of the substrate.

As shown in Figure 1e of Agarwala, there is no via through a printed circuit board. The printed circuit board of the current invention is the substrate through which the via transverses. In Agarwala, the substrate is the layer beneath trace 16 which is shown as solid. The opening in Agarwala is in the passivation layer, not in the substrate. As such, Agarwala does not anticipate Applicants' explicitly claimed invention.

Claim 11 recites similar limitations to those that appear in claim 1. As such, claim 11 is allowable for the same reasons that claim 1 is allowable.

Claims 2-10 depend from, and contain all the limitations of claim 1. These dependent claims also recite additional limitations which, in combination with the limitations of claim 1, are neither disclosed nor suggested by Agarwala and are also directed towards patentable subject matter. Thus, claims 2-10 should be allowed.

Claims 4 and 7 stand rejected under 35 U.S.C. § 103(a) over Agarwala in view of U.S. Patent No. 5,796,589 ("Barrow"). Barrow was not included to solve the deficiencies discussed above but to show a mounting structure of a semiconductor package having vias that correspond to a corner of the semiconductor package. Thus, the objection under 35 U.S.C. § 103 should be withdrawn.

Applicants have responded to all of the rejections and objections recited in the Final Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

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Respectfully submitted,

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